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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,373	12/09/2003	Leendert M. Huisman	BUR920030139US1	1372

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,373	HUISMAN ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 25-31* is/are pending in the application.

4a) Of the above claim(s) *9-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 25-29* is/are rejected.

7)☒ Claim(s) *5-8,30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/9/03 7/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I in the reply filed on 6/19/06 is acknowledged. The traversal is on the ground(s) that there is no serious burden to the examiner. This is not found persuasive because diagnosis of failing scan chains and construction of scan chains have separate classifications which shows that each of Group I and Group II have attained recognition in the art as a separate subject for inventive effort, and also a separate field of search. Therefore, it is necessary to search for one of the inventions in a manner that is not likely to result in finding art pertinent to the other invention. (e.g., searching different classes /subclasses - 714/726 is a different search area than 716/4 - and electronic resources, and employing different search queries), a different field of search is shown. The requirement is still deemed proper and is therefore made FINAL. (MPEP 808.02 [R-3])

Claims 9-20 and 21-24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Group II, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 6/19/06.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims are rejected under 35 U.S.C. 102(e) as being anticipated by Das U.S. Patent No. 6,553,524.

As per claims 1 and 25, Das teaches a system and method for automatic validation during BDL extraction of test hardware of an integrated circuit device. A test hardware portion of connectivity of the integrated circuit device is extracted; electrical and functional validation of the scan latches, test control blocks and test signals of the test hardware is performed during extraction. Following extraction and validation of the test hardware portion, the test hardware portion may be represented in a block description language. Any logged errors, such as test signal connectivity errors, scan latch inter-connectivity errors, etc., that are identified during the extraction and validation process may be used by IC designers to improve the test hardware portion. During the first extraction procedure, the connectivity of test signals, which reside at a number of test signal output ports of a test control block of the test hardware portion having serially-connected scan latch instances, to the serially-connected scan latch instances is determined. Any test signal connectivity errors identified during the first extraction

procedure are generated and logged for future reference (column 3 line 66 through column 4 line 19 Figure 5).

As per claim 2, Das teaches verification of each scan latch (figure 6a element 320).

As per claims 3 and 29, Das teaches that a signal type is assigned to a particular test signal output port of a given test control block of interest. An instance of a number of instances to which a test signal at the particular test signal output port of the test control block will fan (and which is also designated as being traversable) is traversed. This traversal of the instance is used to determine whether the instance is a scan latch instance. Disjointed scan latches are included in the inquiry about whether the instance under scrutiny is a scan latch. Scan latches of the test circuitry can be disjointed if the functional and test portions of the scan latch are representative of two different leaf cells of separate logic that is represented by different artwork that describes the respective circuitries. This is especially of concern in dynamic logic circuits in which the functional piece and the test piece of the scan latch may be separate leaf cells but test signals will still reach the functional leaf cell (column 6 lines 2-20).

As per claim 4, Das teaches the first extraction procedure was concerned with the test signal output ports of a test control block, the second extraction procedure is concerned with the test data output ports of the test control block of interest. A traversable instance of the instances to which a test data signal resident at a test data output port of the test control block will fan to is traversed. An inquiry as to whether the traversal has indicated that the instance is a scan latch instance. If the instance is a

scan latch instance, then the electrical quality of the scan latch instance is checked and any electrical quality errors discovered during the process are logged as failures. The inquiry whether each scan latch port of the scan latch instance has been previously traversed during the first extraction pass. If no, this is indicative of a floating condition, meaning that there is at least one scan latch port that is not connected to a global test signal originating from a TAP or MTAPs. A scan latch port error is generated and logged for each such defective scan latch port (column 7 lines 4-24, Figure 6).

As per claim 26, Das teaches the use of test signals (both global and/or local), that reside at the test signal output ports of a test control block, such as TAP or MTAP, of a given test hardware portion of interest, to serially-connected scan latches (column 5 lines 37-42).

As per claims 27 and 28, Das teaches the first extraction procedure was concerned with the test signal output ports of a test control block, the second extraction procedure is concerned with the test data output ports of the test control block of interest. A traversable instance of the instances to which a test data signal resident at a test data output port of the test control block will fan to is traversed. An inquiry as to whether the traversal has indicated that the instance is a scan latch instance. If the instance is a scan latch instance, then the electrical quality of the scan latch instance is checked and any electrical quality errors discovered during the process are logged as failures. The inquiry whether each scan latch port of the scan latch instance has been previously traversed during the first extraction pass. If no, this is indicative of a floating condition, meaning that there is at least one scan latch port that is not connected to a

global test signal originating from a TAP or MTAPs. A scan latch port error is generated and logged for each such defective scan latch port (column 7 lines 4-24, Figure 6).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"Diagnosing Scan Chain Faults" by Kundu, S. This paper appears in: IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Publication Date: Dec 1994 Volume: 2, Issue: 4 on page(s): 512-516 ISSN: 1063-8210 INSPEC Accession Number: 4839256

This paper teaches a diagnosis system that can diagnose faults in a scan chain. Testing screens for good chips, however, when test fall out is high (low yield) it becomes necessary to diagnose faults so that the manufacturing process or physical design can be filed to improve yield. Several scan based diagnostic schemes are used in industry. These work when the scan chain itself is fault free.

"Scan Chain Diagnosis Using IDDQ Current Measurement" by Hirase et al. This paper appears in: Eighth Asian Test Symposium, 1999. (ATS '99) Proceedings. Publication Date: 1999 on page(s): 153-157 ISBN: 0-7695-0315-2 INSPEC Accession Number: 6544163

This paper teaches for functional failure analysis, use of the scan design for effective testing of sequential circuits is very popular and can be considered the norm for the LSI industry. However, in order to take advantage of the features offered by scan

designs, it is imperative that the scan chain is operating properly. In this paper, It introduces a new technique for the efficient diagnosis of the scan chain. The basis for this paper is that if a failure occurs in the scan chain, irregular IDDQ current flow will occur and identify the defective chain. Moreover, the actual location of the failure inside the chain can also be ascertained.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2138